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L17	1479	hot adj2 insert$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/16 11:59
L18	16605	size adj2 information	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/16 11:59
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L21	373	expandable adj2 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/16 11:59
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1 Pen computing: a technology overview and a vision   ▬
André Meyer
July 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 3

Full text available: 🗎 pdf(5.14 MB)   Additional Information: full citation, abstract, citings, index terms

This work gives an overview of a new technology that is attracting growing interest in public as well as in the computer industry itself. The visible difference from other technologies is in the use of a pen or pencil as the primary means of interaction between a user and a machine, picking up the familiar pen and paper interface metaphor. From this follows a set of consequences that will be analyzed and put into context with other emerging technologies and visions.Starting with a short historic ...

2 Illustrative risks to the public in the use of computer systems and related technology   ▬
Peter G. Neumann
January 1996 **ACM SIGSOFT Software Engineering Notes**, Volume 21 Issue 1

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3 Embedded systems: applications, solutions and techniques (EMBS): An efficient   ▬
management scheme for large-scale flash-memory storage systems
Li-Pin Chang, Tei-Wei Kuo
March 2004 **Proceedings of the 2004 ACM symposium on Applied computing**

Full text available: 🗎 pdf(299.99 KB)   Additional Information: full citation, abstract, references, citings, index terms

Flash memory is among the top choices for storage media in ubiquitous computing. With a strong demand of high-capacity storage devices, the usages of flash memory quickly grow beyond their original designs. The very distinct characteristics of flash memory introduce serious challenges to engineers in resolving the quick degradation of system performance and the huge demand of main-memory space for flash-memory management when high-capacity flash memory is considered. Although some brute-force so ...

Keywords: consumer electronics, embedded systems, flash memory, memory management, portable devices, storage systems

4 Illustrative risks to the public in the use of computer systems and related technology   ▬

Peter G. Neumann
January 1992 **ACM SIGSOFT Software Engineering Notes**, Volume 17 Issue 1

Full text available: ⬛ pdf(1.65 MB)   Additional Information: full citation, citings, index terms

5 An efficient r-tree implementation over flash-memory storage systems   ▬

Chin-Hsien Wu, Li-Pin Chang, Tei-Wei Kuo
November 2003 **Proceedings of the 11th ACM international symposium on Advances in geographic information systems**

Full text available: ⬛ pdf(190.75 KB)   Additional Information: full citation, abstract, references, citings, index terms

For many applications with spatial data management such as Geographic Information Systems (GIS), block-oriented access over flash memory could introduce a significant number of node updates. Such node updates could result in a large number of out-place updates and garbage collection over flash memory and damage its reliability. In this paper, we propose a very different approach which could efficiently handle fine-grained updates due to R-tree index access of spatial data over flash memory. The ...

Keywords: GIS, R-tree, embedded systems, flash memory, spatial index structures, storage systems

6 Very rapid prototyping of wearable computers: a case study of custom versus off-the-   ▬
shelf design methodologies

Asim Smailagic, Daniel P. Siewiorek, Richard Martin, John Stivoric
June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: ⬛ pdf(121.36 KB)   Additional Information: full citation, abstract, references, citings, index terms
⬛ Publisher Site

The Wearable Computer Project is a testbed integratingresearch on rapid design and prototyping. Based onrepresentative examples from six generations of wearablecomputers, the paper focuses on the differences in rapidprototyping using custom design versus off-the-shelfcomponents. The attributes characterizing these two designstyles are defined and illustrated by experimentalmeasurements. The off-the-shelf approach required ten timesthe overhead, 30% more cost, fifty times the storage resources,20 ...

7 Energy-aware design of embedded memories: A survey of technologies, architectures,   ▬
and optimization techniques

Luca Benini, Alberto Macii, Massimo Poncino
February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Full text available: ⬛ pdf(288.44 KB)   Additional Information: full citation, abstract, references, index terms

Embedded systems are often designed under stringent energy consumption budgets, to limit heat generation and battery size. Since memory systems consume a significant amount of energy to store and to forward data, it is then imperative to balance power consumption and performance in memory system design. Contemporary system design focuses on the trade-off between performance and energy consumption in processing and storage units, as well as in their interconnections. Although memory design is as ...

Keywords: Embedded systems, embedded memories, integration, memories, nonvolatile, system-on-a-chip, volatile

8 Interaction design at the Utrecht School of the Arts

Lon Barfield, Willie van Burgsteden, Ruud Lanfermeijer, Bert Mulder, Jurriënne Ossewold, Dick
Rijken, Philippe Wegner
July 1994 **ACM SIGCHI Bulletin**, Volume 26 Issue 3

Full text available: pdf(5.38 MB)   Additional Information: full citation, abstract, citings, index terms

> The "Hogeschool voor de Kunsten Utrecht" (Utrecht School of the Arts, Utrecht, The
> Netherlands) offers a four-year curriculum in interaction design (roughly equivalent to an
> MA) and a one year master of arts degree in interactive multimedia. The material here
> presents our approach to interaction design as a discipline and the curriculum that embodies
> this approach. It features a collection of thoughts and snapshots-- we regard it as work in
> progress. Interaction design is a new field. It is grow ...

9 TILT: Translation in Leisure Time

Abby Gelles, Gary Harris
September 1980 **Proceedings of the 3rd ACM SIGSMALL symposium and the first SIGPC
symposium on Small systems**

Full text available: pdf(676.73 KB)   Additional Information: full citation, abstract, references, index terms

> This paper addresses the question whether it is feasible to implement a computerized
> translation between audio-visual equipment-driving programmers. Programmer systems are
> comprised of the hardware and software components which record and play back coded cues
> defining audio-visual presentation sequences. Cue sequence output differs between
> programmer systems in the actual coding schemes attributed to cues, the number
> contiguous of repetitions per cue (redundancy factor) in the output stream ...

> **Keywords**: Audio-visual programmer, Cue bit stream, Leisure time

10 IS '97: model curriculum and guidelines for undergraduate degree programs in
information systems

Gordon B. Davis, John T. Gorgone, J. Daniel Couger, David L. Feinstein, Herbert E.
Longenecker
December 1996 **ACM SIGMIS Database , Guidelines for undergraduate degree programs
on Model curriculum and guidelines for undergraduate degree
programs in information systems**, Volume 28 Issue 1

Full text available: pdf(7.24 MB)   Additional Information: full citation, citings

11 OMP: a RISC-based multiprocessor using orthogonal-access memories and multiple
spanning buses

K. Hwang, M. Dubois, D. K. Panda, S. Rao, S. Shang, A. Uresin, W. Mao, H. Nair, M. Lytwyn, F.
Hsieh, J. Liu, S. Mehrotra, C. M. Cheng
June 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 4th
international conference on Supercomputing**, Volume 18 Issue 3

Full text available: pdf(1.96 MB)   Additional Information: full citation, abstract, references, citings, index
terms

> This paper presents the architectural design and RISC based implementation of a prototype
> supercomputer, namely the Orthogonal MultiProcessor (OMP). The OMP system is
> constructed with 16 Intel 1860 RISC microprocessors and 256 parallel memory modules,
> which are 2-D interleaved and orthogonally accessed using custom-designed spanning
> buses. The architectural design has been validated by a CSIM-based multiprocessor
> simulator. The design choices are based on worst-case delay a ...

12 Link and channel measurement: A simple mechanism for capturing and replaying wireless channels

Glenn Judd, Peter Steenkiste

August 2005 **Proceeding of the 2005 ACM SIGCOMM workshop on Experimental approaches to wireless network design and analysis E-WIND '05**

Full text available: pdf(6.06 MB)   Additional Information: full citation, abstract, references, index terms

Physical layer wireless network emulation has the potential to be a powerful experimental tool. An important challenge in physical emulation, and traditional simulation, is to accurately model the wireless channel. In this paper we examine the possibility of using on-card signal strength measurements to capture wireless channel traces. A key advantage of this approach is the simplicity and ubiquity with which these measurements can be obtained since virtually all wireless devices provide the req ...

Keywords: channel capture, emulation, wireless

13 UTLB: a mechanism for address translation on network interfaces

Yuqun Chen, Angelos Bilas, Stefanos N. Damianakis, Cezary Dubnicki, Kai Li

October 1998 **Proceedings of the eighth international conference on Architectural support for programming languages and operating systems**, Volume 33 , 32 Issue 11 , 5

Full text available: pdf(1.76 MB)   Additional Information: full citation, abstract, references, citings, index terms

An important aspect of a high-speed network system is the ability to transfer data directly between the network interface and application buffers. Such a *direct data path* requires the network interface to "know" the virtual-to-physical address translation of a user buffer, *i.e.*, the physical memory location of the buffer. This paper presents an efficient address translation architecture, User-managed TLB (UTLB), which eliminates system calls and device interrupts from the common co ...

14 Options for dynamic address translation in COMAs

Xiaogang Qiu, Michel Dubois

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

Full text available: pdf(1.37 MB) Publisher Site   Additional Information: full citation, abstract, references, citings, index terms

In modern processors, the dynamic translation of virtual addresses to support virtual memory is done before or in parallel with the first-level cache access. As processor technology improves at a rapid pace and the working sets of new applications grow insatiably the latency and bandwidth demands on the TLB (Translation Lookaside Buffer) are getting more and more difficult to meet. The situation is worse in multiprocessor systems, which run larger applications and are plagued by the TLB consiste ...

15 Structured machine design: An ongoing experiment

Richard F. Hobson

May 1981 **Proceedings of the 8th annual symposium on Computer Architecture**

Full text available: pdf(872.83 KB)   Additional Information: full citation, abstract, references, citings, index terms

In the following sections, the needs of structured architecture from the point of view of a single-user HLLCS is discussed. A prototype machine is introduced, and its design is treated as an ongoing experiment in structured machine design. This approach is relevant because historical evidence suggests that computer architecture (hardware and software) evolves slowly, requiring valuable information obtained through everyday use.

16 eNVy: a non-volatile, main memory storage system

Michael Wu, Willy Zwaenepoel

November 1994 **Proceedings of the sixth international conference on Architectural support for programming languages and operating systems**, Volume 29 , 28 Issue 11 , 5

Full text available: pdf(1.32 MB)   Additional Information: full citation, abstract, references, citings, index terms

This paper describes the architecture of eNVy, a large non-volatile main memory storage system built primarily with Flash memory. eNVy presents its storage space as a linear, memory mapped array rather than as an emulated disk in order to provide an efficient and easy to use software interface.Flash memories provide persistent storage with solid-state memory access times at a lower cost than other solid-state technologies. However, they have a number of drawbacks. Flash chips are ...

17 Integration of message passing and shared memory in the Stanford FLASH multiprocessor

John Heinlein, Kourosh Gharachorloo, Scott Dresser, Anoop Gupta

November 1994 **Proceedings of the sixth international conference on Architectural support for programming languages and operating systems**, Volume 29 , 28 Issue 11 , 5

Full text available: pdf(1.80 MB)   Additional Information: full citation, abstract, references, citings, index terms

The advantages of using message passing over shared memory for certain types of communication and synchronization have provided an incentive to integrate both models within a single architecture. A key goal of the FLASH (FLexible Architecture for SHared memory) project at Stanford is to achieve this integration while maintaining a simple and efficient design. This paper presents the hardware and software mechanisms in FLASH to support various message passing protocols. We achieve low overhe ...

18 Papers: Wireless data communications using DECT air interface

António Muchaxo, Alexandre Sousa, Nuno Pereira, Helena Sarmento

April 1999 **ACM SIGCOMM Computer Communication Review**, Volume 29 Issue 2

Full text available: pdf(1.25 MB)   Additional Information: full citation, abstract, references, citings

DECT is an approved ETSI standard for cordless communications, defined as a general radio access technology that can be used as the air interface to any network. In addition to the well-established voice service, it supports data communications. DECT currently addresses low bit rates, but additional modulation options have recently been included for high-speed, up to 2Mbps. In this paper, we describe the hardware and software design of an entire wireless communications system to be used in SOHO ...

19 Security as a new dimension in embedded system design: Security as a new dimension in embedded system design

Srivaths Ravi, Paul Kocher, Ruby Lee, Gary McGraw, Anand Raghunathan

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(209.10 KB)   Additional Information: full citation, abstract, references, citings, index terms

The growing number of instances of breaches in information security in the last few years has created a compelling case for efforts towards secure electronic systems. Embedded systems, which will be ubiquitously used to capture, store, manipulate, and access data of a sensitive nature, pose several unique and interesting security challenges. Security has been the subject of intensive research in the areas of cryptography, computing, and networking. However, despite these efforts, *security is* ...

Keywords: PDAs, architectures, battery life, cryptography, design, design methodologies, digital rights management, embedded systems, performance, security, security processing, security protocols, sensors, software attacks, tamper resistance, trusted computing, viruses

20 Measuring experimental error in microprocessor simulation

Rajagopalan Desikan, Doug Burger, Stephen W. Keckler

May 2001   **ACM SIGSOFT Software Engineering Notes , Proceedings of the 2001 symposium on Software reusability: putting software reuse in context**, Volume 26 Issue 3

Full text available: pdf(1.03 MB)   Additional Information: full citation, references, index terms

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